

**REMARKS**

Claims 19-28, 30, 31, 33-37 and 39-41 are pending in this application. Claims 19, 31 and 40 have been amended. Claim 32 has been canceled and its limitations have been incorporated in amended independent claim 31.

Claims 19, 21, 22, 24, 25, 28, 30, 31, 33, 34, 37 and 39-41 stand rejected under 35 U.S.C. §102 as being anticipated by Anand (U.S. Patent No. 6,362,528) (“Anand”). This rejection is respectfully traversed.

The claimed invention relates to a dual damascene structure comprising a titanium-silicon-nitride layer. As such, amended independent claim 19 recites a “dual damascene structure” comprising *inter alia* a metal layer “provided within” a first insulating layer, “a second insulating layer provided over said metal layer” and “a via situated within said second insulating layer and . . . lined with an organo-metallic-atomic deposited titanium-silicon-nitride layer and filled with a copper material.” Amended independent claim 19 also recites a trench situated within a third insulating layer and “lined with said organo-metallic-atomic deposited titanium-silicon-nitride layer and filled with said copper material.”

Amended independent claim 31 recites a “damascene structure” comprising *inter alia* a semiconductor substrate, “a metal layer provided within” a first insulating layer and “at least another insulating layer provided over said metal layer.” Amended independent claim 31 also recites “at least one opening situated within said at least another insulating layer and . . . lined with a titanium-silicon-nitride layer and filled with a copper material.” Amended independent claim 31 further recites that the “another insulating layer” includes “a material selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene, SILK, fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLASS.”

Amended independent claim 40 recites “a damascene structure” which is part of

a processor-based system and which comprises *inter alia* “a metal layer provided within a first insulating layer” and “at least another insulating layer provided over said metal layer.” Amended independent claim 40 also recites “at least one opening situated within said at least another insulating layer and . . . lined with an organo-metallic-atomic deposited titanium-silicon-nitride layer and filled with copper.”

Anand relates to a “bonding pad . . . formed in a lattice-like shape.” (Abstract). According to Anand, the bonding pad is “constituted by a conductive member filled in grooves made in an insulating layer having a flat surface.” (Col. 7, lines 26-28). Anand also teaches “an etching stopper layer formed on the insulating layer and having an opening to expose the bonding pad” and “a passivation layer formed on the etching stopper layer and having an opening to expose the bonding pad.” (Col. 7, lines 28-33). In this manner, “[W]ith this structure, the bonding error of the device manufactured by the damascening process can be avoided.” (Abstract).

Anand does not disclose all limitations of claims 19, 21, 22, 24, 25, 28, 30, 31, 33, 34, 37 and 39-41. Anand does not teach or disclose a “dual damascene structure” comprising *inter alia* “a via situated within said second insulating layer and . . . lined with an *organo-metallic-atomic deposited titanium-silicon-nitride layer* and filled with a copper material,” as amended independent claims 19 and 40 recite (emphasis added). Anand is also silent about a “damascene structure” comprising *inter alia* “another insulating layer” including “a material selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene, SILK, fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLASS,” as amended independent claim 31 recites. In describing the formation of the bonding pad, Anand teaches that “barrier metal 20a is formed in the insulating layer 27, on the inner surface of the contact hole 19a and the inner surfaces of the grooves 19b and 19b’” (col. 13, lines 8-11; Figure 37, 38) “of, for example, a lamination of titanium and titanium nitride, or silicon titanium nitride, or the like.” (Col. 13, lines 11-13). In Anand, however, barrier metal layer 20a is formed “by the CVD method or PVD method” (col. 13, lines 8-11;

Figure 37, 38), and not by organo-metallic atomic layer deposition, as in the claimed invention. Anand further teaches that the insulating layer 27 “is made of, for example, silicon oxide” (col. 12, lines 41-42), and not of the materials recited in amended independent claim 31. Accordingly, Anand does not disclose the limitations of claims 19, 21, 22, 24, 25, 28, 30, 31, 33, 34, 37 and 39-41, and withdrawal of the rejection of these claims is respectfully requested.

Claims 20 and 23 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Anand in view of Venkatraman et al. (U.S. Patent No. 6,093,966) (“Venkatraman”). This rejection is respectfully traversed.

Claims 20 and 23 depend on amended independent claim 19 and recite that each of the first and second insulating layers “includes a material selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene, SILK, fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLOSS.”

Venkatraman relates to an interconnect structure comprising a copper barrier layer that prevents silicon enrichment at the bottom of such structure. (Abstract; Col. 12-16). Venkatraman teaches openings 195, 196 formed within a first and second insulating layers 180, 190 and provided with copper barrier layers 200, 201 having different silicon concentrations. (Abstract; Figures 9-10). Venkatraman notes that copper barrier layer 200 (201) “is typically a tantalum silicon nitride layer, but may also be composed of any combination of refractory metal such as molybdenum, tungsten, titanium, vanadium together with silicon and nitrogen (e.g. a nitrogen-containing tantalum).” (Col. 5, lines 22-27).

The subject matter of claims 20 and 23 would not have been obvious over Colgan in view of Venkatraman. Indeed, the Office Action fails to establish a *prima facie* case of obviousness. Courts have generally recognized that a showing of a *prima facie* case of obviousness necessitates three requirements: (i) some suggestion or motivation, either

in the references themselves or in the knowledge of a person of ordinary skill in the art, to modify the reference or combine the reference teachings; (ii) a reasonable expectation of success; and (iii) the prior art references must teach or suggest all claim limitations. See e.g., In re Dembiczak, 175 F.3d 994, 50 U.S.P.Q.2d 1614 (Fed. Cir. 1999); In re Rouffet, 149 F.3d 1350, 1355, 47 U.S.P.Q.2d 1453, 1456 (Fed. Cir. 1998); Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc., 75 F.3d 1568, 1573, 37 U.S.P.Q.2d 1626, 1630 (Fed. Cir. 1996).

In the present case, neither Anand nor Venkatraman, whether considered alone or in combination, teaches or suggests the limitations of claims 20 and 23. Anand fails to teach or suggest a “dual damascene structure” comprising “a via situated within said second insulating layer and . . . lined with an organo-metallic-atomic deposited titanium-silicon-nitride layer and filled with a copper material,” as amended independent claim 19 recites. Similarly, Venkatraman does not teach or suggest all limitations of amended independent claim 19. Venkatraman fails to teach or suggest a “damascene structure” comprising a substrate and “a via” situated over “a metal layer provided within a first insulating layer,” as amended independent claim 19 recites. Venkatraman teaches openings 195, 196 formed within a first and second insulating layers 180, 190 and provided with copper barrier layers 200, 201 having different silicon concentrations. (Abstract; Figures 9-10). In Venkatraman, however, metal layer 170 is not provided within an insulating layer, as in the claimed invention.

Claims 26, 27, 35 and 36 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Anand and Venkatraman in further view of *Ti-Si-N Diffusion Barriers Between Silicon and Copper* by J.S. Reid et al. (“Reid”). This rejection is respectfully traversed.

Reid teaches a 10nm (100 Angstroms) titanium silicon nitrogen barrier layer between a silicon substrate and a copper overlayer. Because none of Anand, Venkatraman and Reid teaches or suggests the limitations of amended independent claims 19, 31 and 40, the subject matter of claims 26, 27, 35 and 36 would not have been obvious over Anand

and Venkatraman in view of Reid, and withdrawal of the rejection of these claims is also respectfully requested.

A marked-up version of the changes made to the specification and claims by the current amendment is attached. The attached page is captioned "**Version with markings to show changes made.**"

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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**Version With Markings to Show Changes Made**

19. (twice amended) A dual damascene structure comprising:

a semiconductor substrate;

a first insulating layer provided over said semiconductor substrate;

a metal layer provided within said first insulating layer;

a second insulating layer provided over said metal layer;

a via situated within said second insulating layer and extending to at least a portion of said metal layer, said via being lined with [a] an organo-metallic-atomic deposited titanium-silicon-nitride layer and filled with a copper material;

a third insulating layer located over said second insulating layer;

a trench situated within said third insulating layer and extending to said via, said trench being lined with said organo-metallic-atomic deposited titanium-silicon-nitride layer and filled with said copper material.

31. (twice amended) A damascene structure comprising:

a semiconductor substrate;

a first insulating layer provided over said semiconductor substrate;

a metal layer provided within said first insulating layer;

at least another insulating layer provided over said metal layer [includes], said at least another insulating layer including a material selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene, SILK, fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLASS; and

at least one opening situated within said at least another insulating layer and extending to at least a portion of said metal layer, said opening being lined with a titanium-silicon-nitride layer and filled with a copper material.

40. (twice amended) A processor-based system comprising:

a processor; and

an integrated circuit coupled to said processor, at least one of said processor and integrated circuit including a damascene structure, said damascene structure comprising a metal layer provided within a first insulating layer formed over a substrate, at least another insulating layer provided over said metal layer, and at least one opening situated within said at least another insulating layer and extending to at least a portion of said metal layer, said opening being lined with [a] an organo-metallic-atomic deposited titanium-silicon-nitride layer and filled with copper.